



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yeo, *et al.*

Attorney Docket: TSM03-0421

Filed: June 27, 2003

Examiner: TBD

Serial No.: 10/608,287

Art Unit: 2812

For: Structure and Method for Forming the Gate Electrode in a Multiple-Gate Transistor

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO-1449 that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

Ira S. Matsil
Attorney for Applicant
Reg. No. 35,272

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
(972) 732-1001 (phone)
(972) 732-9218 (fax)



PTO/SB/08B (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449B/PTO				Complete if Known	
				Application Number	10/608,287
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	June 27, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Group Art Unit	2812
				Examiner Name	TBD
Sheet	2	of	2	Attorney Docket Number	TSM03-0421

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	J	HUANG, X., <i>et al.</i> "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5 (May 2001) pp. 880-886.	
	K	YANG, F.-L., <i>et al.</i> "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, (June 2002) pp. 109-110.	
	J	WONG, H.-S.P. "Beyond the Conventional Transistor," IBM Journal of Research and Development, Vol. 46, No. 2/3 (March/May 2002) pp. 133-167.	
	L	CHAU, R., <i>et al.</i> "Advanced Depleted-Substrate Transistors: Single-gate, Double-Gate and Tri-Gate," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, (2002) pp. 68-69.	
	M	YANG, F.-L., <i>et al.</i> "25nm CMOS Omega FETs," International Electron Devices Meeting, Digest of Technical Papers, (December 2002) pp. 255-258.	
	N	COLINGE, J.P., <i>et al.</i> "Silicon-On-Insulator 'Gate -All-Around Device,'" International Electron Devices Meeting, (1990) pp. 595-598.	
	O	LEOBANDUNG, E., <i>et al.</i> "Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Channel Effects," Journal of Vacuum Science and Technology, Vol. B 15, No. 6, (November/December 1997) pp. 2791-2794.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached. Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.